G0949

COMPOSITE SPACER LINER FOR IMPROVED TRANSISTOR PERFORMANCE

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TECHNICAL FIELD

The present invention relates to a semiconductor device having improved transistor performance and enabling methodology. The present invention has particular applicability in fabricating high density semiconductor devices with high speed integrated circuits having submicron design features and shallow junction depths.

BACKGROUND ART

The escalating demand for high density and performance impose severe requirements on semiconductor fabrication technology, particularly for enhanced transistor performance and high operating speed. Transistor performance depends upon various factors and can easily be degraded by various processing operations during fabrication, such as plasma deposition techniques wherein the substrate is exposed to high temperatures and plasmas, as during plasma enhanced chemical vapor deposition. The need for high operating speed also requires the use of dielectric materials having a relatively low dielectric constant, such as about 3.9 or less. The value of a dielectric constant (k) expressed herein is based upon the value of 1 for a vacuum.

In implementing conventional fabrication techniques, as illustrated in Fig. 1, a gate electrode 11 is typically formed over a semiconductor substrate 10 with a gate dielectric layer 12, e.g., gate oxide layer, therebetween. Ion implantation is then conducted to implant shallow source/drain extensions 13. An oxide liner 15 is then formed on side surfaces of gate electrode 11 and the upper surface of substrate 10, as at a thickness of about 50 Å to about 200 Å to protect the substrate surface during subsequent etching to form sidewall spacers 16, typically formed of silicon nitride. Reference character 14 illustrates a moderate or heavy doped source/drain region typically implanted subsequent to forming sidewall spacers 16.

Difficulties are encountered in implementing conventional semiconductor fabrication techniques, such as those used to form the structure illustrated in Fig. 1. For example, during high temperature processing, as during deposition of the silicon oxide liner 15 by low pressure chemical vapor deposition, typically at a temperature of about 700°C or higher, dopant impurities implanted into the source/drain extensions 13, such as P-type impurities, particularly boron (B) impurities, diffuse and segregate in the oxide liner 15. Such diffusion loss from the source/drain extensions are